H2B2VS
D4.2.2

Final Publication Report

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EXECUTIVE SUMMARY

This deliverable provides a summary of all the publications produced by the project partners in relation to the project related activities. Publications include papers submissions to journals, international conferences, workshops and any other events publishing peer-reviewed proceedings.
The project partners targeted high-impact conferences and journals such as those sponsored by the IEEE and ACM associations. Other highly visible events were targeted as well such as the International Broadcasting Conference (IBC) and the NAB Show, the two largest worldwide events on professional broadcasting.
Other publications are related to national events focusing on the latest technology and solutions concerning broadcasting and multimedia streaming. Events focusing on media synchronisation – a topic of increasing interest for the industry - were addressed as well in 2013 and 2015.
At the moment of editing this document a total of 31 publications were submitted to journals, conferences, exhibitions and other events with the following outcome:

- Submitted: 31
- Accepted: 25
- Pending: 3
- Rejected: 3

This report provides a list of the publications with the relevant details and an abstract. All the papers are available for free download on the project web site: http://h2b2vs.epfl.ch
The document has been periodically updated with all the publications produced during the project lifetime.

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1 DOCUMENT HISTORY AND ABBREVIATIONS

1.1 Document history

Version	Date	Description of the modifications
0.1	29/06/2015	First Revision
0.2	30/06/2015	Revisions from TUT and TVN
1.0	17/08/2015	Final Revision
1.1	23/09/2015	Further revision with additional feedback from partners

1.2 Abbreviations

DSP	Digital Signal Processor
HD	High Definition
HEVC	High Efficiency Video Coding
ICIP	IEEE International Conference on Image Processing
ICASSP	International Conference on Acoustics, Speech, and Signal Processing
ICCE	IEEE Conference on Consumer Electronics
NAB	National Association of Broadcasters
RVC	Reconfigurable Video Coding
SD	Standard Definition
SHVC	Scalable high efficiency video coding
TCSVT	Transactions on Circuits and Systems for Video Technology
UHD	Ultra High Definition

2 PUBLICATIONS SUMMARY

This section lists the project publications with the related status. Of the 31 publications submitted 25 were accepted, 3 rejected and 3 are still under review. Papers with status "accepted" are not publicly available yet but authors have been notified of acceptance.

2.1 Journals

Journal	Title	Authors	Issue/Date	Status
IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS FOR VIDEO TECHNOLOGY	EFFICIENT MODE DECISION SCHEMES FOR HEVC INTER PREDICTION	J. VANNE, M. VIITANEN, T. D. HÄMÄLÄINEN	SEPTEMBER 2014 PP. 1579 - 1593	PUBLISHED
IEEE TRANSACTIONS ON CONSUMER ELECTRONICS	COMPLEXITY ANALYSIS OF AN HEVC DECODER BASED ON A DIGITAL SIGNAL PROCESSOR	PESCADOR, F.; CHAVARRIAS, M.; GARRIDO, M.J.; JUAREZ, E.; SANZ, C.	VOL. 59; ISSUE 2; PP. 391-399; MAY 2013	PUBLISHED
IEEE TRANSACTIONS ON CONSUMER ELECTRONICS	A DSP-BASED HEVC DECODER IMPLEMENTATION USING AN ACTOR LANGUAGE DATAFLOW MODEL	CHAVARRIAS, M.; PESCADOR, F. ; GARRIDO, M. ; JUÁREZ, E. ; RAULET, M.	VOL. 59; ISSUE 4; PP. 839-847; NOV 2013	PUBLISHED
IEEE TRANSACTION ON CONSUMER ELECTRONICS	A MULTICORE DSP HEVC DECODER USING AN ACTOR-BASED DATAFLOW MODEL AND OPENMP	CHAVARRIAS, M. ; PESCADOR, F. ; GARRIDO, M.J. ; JUAREZ, E. ; SANZ, C.	9-12 JAN. 2015. PP. 370 - 371	PUBLISHED
JOURNAL OF REAL-TIME IMAGE PROCESSING (JRTIP), 2015	LOW POWER HEVC SOFTWARE DECODER FOR MOBILE DEVICES	RAFFIN E.; NOGUES E.; HAMIDOUCHE W.; TOMPERI S. ; PELCAT M. ; MENARD D.	JUNE 2015	ACCEPTED
IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS FOR VIDEO TECHNOLOGY	4K REAL-TIME AND PARALLEL SOFTWARE VIDEO DECODER FOR MULTI-LAYER HEVC EXTENSIONS	HAMIDOUCHE W., RAULET, M., DEFORGES, O.	TBD	ACCEPTED
ICISC 2015 – 18TH ANNUAL INTERNATIONAL CONFERENCE ON INFORMATION SECURITY AND CRYPTOLOGY	CIPHERTEXT-POLICY ATTRIBUTE-BASED BROADCAST ENCRYPTION WITH SMALL KEYS	WESOLOWSKI B; JUNOD P.		SUBMITTED
IEEE CIRCUIT AND SYSTEMS FOR VIDEO TECHNOLOGY	A MULTICORE DSP HEVC DECODER USING AN ACTOR-BASED DATAFLOW MODEL			REJECTED

Table 1 - Journals publications

2.2 Conferences

Conferences	Title	Authors	Issue/Date	
ICCE 2014 - IEEE CONFERENCE ON CONSUMER ELECTRONICS	ON AN IMPLEMENTATION OF HEVC VIDEO DECODERS WITH DSP TECHNOLOGY	PESCADOR, F.; GARRIDO, M.J.; JUAREZ, E.; SANZ, C.	JANUARY 2014 PP. 121-122	PUBLISHED
ICCE 2014 - IEEE CONFERENCE ON CONSUMER ELECTRONICS	A DSP HEVC DECODER IMPLEMENTATION BASED ON OPENHEVC	F. PESCADOR, J. P. CAÑO, M.J. GARRIDO, E. JUAREZ AND M. RAULET	JANUARY 2014 PP. 61 – 62	PUBLISHED
ICASSP 2014 – IEEE - INTERNATIONAL CONFERENCE ON ACOUSTICS, SPEECH, AND SIGNAL PROCESSING	MULTI-CORE SOFTWARE ARCHITECTURE FOR THE SCALABLE HEVC DECODER	HAMIDOUCHE W., RAULET, M., DEFORGES, O.	MAY 2014 PP. 7545 - 7549	PUBLISHED
DASIP 2014 - CONFERENCE ON DESIGN & ARCHITECTURES FOR SIGNAL & IMAGE PROCESSING	MPEG HIGH EFFICIENT VIDEO CODING STREAM PROGRAMMING AND MANY-CORES SCALABILITY	DE SAINT JORRE .; RENZI D.; CASALE BRUNET S.; WISZNIEWSKA M.; BEZATI E.; MATTAVELLI M.	SEPTEMBER 2014	PUBLISHED
ICIP 2014 - IEEE INTERNATIONAL CONFERENCE ON IMAGE PROCESSING	EXPLORING MPEG HEVC DECODER PARALLELISM FOR THE EFFICIENT PORTING ONTO MANY-CORE PLATFORMS	D. DE SAINT JORRE, C. ALBERTI, M. MATTAVELLI, S. CASALE-BRUNET	OCTOBER 2014 PP. 2115 - 2119	PUBLISHED
ICIP 2014 - IEEE INTERNATIONAL CONFERENCE ON IMAGE PROCESSING	REAL TIME SHVC DECODER: IMPLEMENTATION AND COMPLEXITY ANALYSIS	HAMIDOUCHE, W. ; RAULET, M. ; DEFORGES, O.	OCTOBER 2014 PP. 2125 - 2129	PUBLISHED
ICME 2014 – IEEE CONFERENCE ON MULTIMEDIA & EXPO	PARALLEL SHVC DECODER: IMPLEMENTATION AND ANALYSIS	W. HAMIDOUCHE, M. RAULET AND O. DEFORGES	JULY 14-18, 2014	PUBLISHED
SIPS 2014 - IEEE WORKSHOP ON SIGNAL PROCESSING SYSTEMS	DATAFLOW PROGRAMS ANALYSIS AND OPTIMIZATION USING	CANALE, M. ; CASALE-BRUNET, S. ; BEZATI, E. ; MATTAVELLI, M. ;	OCTOBER 2014 PP 1-6	PUBLISHED

	MODEL PREDICTIVE CONTROL TECHNIQUES	JANNECK, J.W.		
VCIP 2014 – IEEE VISUAL COMMUNICATIONS AND IMAGE PROCESSING CONFERENCE	COMPARATIVE STUDY OF 8 AND 10-BIT HEVC ENCODERS	VANNE, J. ; VIITANEN, M. ; KOIVULA, A. ; HÄMÄLÄINEN, T.D.	DECEMBER 2014 PP. 542 - 545	PUBLISHED
IEEE INTERNATIONAL SYMPOSIUM ON CONSUMER ELECTRONICS 2015	A DSP-BASED HEVC DECODER IMPLEMENTATION USING RVC-CAL AND NATIVE OPENHEVC CODE	RODRIGUEZ, P.; BALSEIRO, F.; CHAVARRIAS, M.; PESCADOR, F.; GARRIDO, M.	JUNE 2015	ACCEPTED
ISCAS 2015 – IEEE INTERNATIONAL SYMPOSIUM ON CIRCUITS AND SYSTEMS	KVAZAAR HEVC ENCODER FOR EFFICIENT INTRA CODING	M. VIITANEN, A. KOIVULA, A. LEMMETTI, J. VANNE, T. D. HÄMÄLÄINEN	MAY 2015	PUBLISHED
SPRO 2015 – IEEE/ACM 1ST INTERNATIONAL WORKSHOP ON SOFTWARE PROTECTION	OBFUSCATOR-LLVM – SOFTWARE PROTECTION FOR THE MASSES	JUNOD P.; RINALDINI J.; WEHRLI J.;MICHIELIN J.	MAY 2015	PUBLISHED
ICCE 2015 - IEEE CONFERENCE ON CONSUMER ELECTRONICS	A MULTICORE DSP HEVC DECODER USING AN ACTOR-BASED DATAFLOW MODEL	CHAVARRIAS, M.; PESCADOR, F.; GARRIDO, M.J.; JUAREZ, E.; SANZ, C.	YEAR: 2015 PAGES: 370 - 371	PUBLISHED
IEEE GLOBECOM 2015	NETWORK-ASSISTED MULTIPATH DASH USING THE DISTRIBUTED DECISION ENGINE			SUBMITTED
SIPS 2015 – IEEE INTERNATIONAL WORKSHOP ON SIGNAL PROCESSING SYSTEMS	PARALLELIZATION OF KVAZAAR HEVC INTRA ENCODER FOR MULTI-CORE PROCESSORS	A. KOIVULA, M. VIITANEN, J. VANNE, T. D. HÄMÄLÄINEN, L. FASNACHT		SUBMITTED
ACM CONFERENCE ON COMPUTER AND COMMUNICATIONS SECURITY	CIPHERTEXT-POLICY ATTRIBUTE-BASED BROADCAST ENCRYPTION WITH SMALL KEYS	WESOLOWSKI B; JUNOD P.		REJECTED

Table 2 - Conferences publications

2.3 Other events

Other Events	Title	Authors	Issue/Date	
MEDIA SYNCHRONIZATION WORKSHOP 2013	HYBRID BROADCAST SERVICES USING MPEG DASH	JEAN LE FEUVRE AND CYRIL CONCOLATO	OCTOBER 29, 2013, NANTES, FRANCE	ACCEPTED
NAB SHOW 2014	4K ARRIVES! A PERSPECTIVE FROM A REAL UHDTV BROADCASTING EXPERIENCE	MOURELLE, A.; RODRIGUEZ, J. ; SANZ, I.	9TH APRIL 2014	ACCEPTED
FOURTH W3C WEB AND TV WORKSHOP	HYBRID TELEVISION - USE CASES AND BUSINESS MODELS PROPOSED BY THE H2B2VS PROJECT	RAOUL MONNIER	12-13 MARCH 2014	ACCEPTED
MEDIA SYNCHRONIZATION WORKSHOP 2015	A TEST BED FOR HYBRID BROADCAST BROADBAND SERVICES	LE FEUVRE J.; NGUYEN V.; HAMMIDOUCHE W. ; MARCHAL P. ; MONNIER R. ; DUPAIN P.	JUNE 2015	ACCEPTED
IBC 2015	H2B2VS (HEVC HYBRID BROADCAST BROADBAND VIDEO SERVICES) – BUILDING INNOVATIVE SOLUTIONS OVER HYBRID NETWORKS	MONNIER R. ; MOURELLE A. ; ALBERTI C. ; BERNOUX J-P. ; LE FEUVRE J.	SEPTEMBER 2015	ACCEPTED
LP-EMS15 - WORKSHOP ON DESIGN OF LOW POWER EMBEDDED MULTIMEDIA SYSTEMS	ENERGY EFFICIENCY OF A PARALLEL HEVC SOFTWARE DECODER FOR EMBEDDED DEVICES	RAFFIN E.; NOGUES E.; HAMIDOUCHE W.; TOMPERI S. ; PELCAT M. ; MENARD D.	MAY 2015	PUBLISHED
ESTIMEDIA 2013 WORKSHOP	A DSP HEVC DECODER IMPLEMENTATION BASED ON A RVC-CAL DATAFLOW MODEL	CHAVARRIAS, M.; PESCADOR, F. ; GARRIDO, M. ; JUÁREZ, E. ; RAULET, M.	--	REJECTED

Table 3 - Project publications to other events

3 JOURNALS

3.1 IEEE Transactions on Circuits and Systems for Video Technology

3.1.1 Efficient Mode Decision Schemes for HEVC Inter Prediction (2014)

The emerging High Efficiency Video Coding (HEVC) standard reduces the bit rate by almost 40% over the preceding state-of-the-art Advanced Video Coding (AVC) standard with the same objective quality but at about 40% encoding complexity overhead. The main reason for HEVC complexity is inter prediction that accounts for 60%-70% of the whole encoding time. This paper analyzes the rate-distortion-complexity characteristics of the HEVC inter prediction as a function of different block partition structures and puts the analysis results into practice by developing optimized mode decision schemes for the HEVC encoder. The HEVC inter prediction involves three different partition modes: square motion partition, symmetric motion partition (SMP), and asymmetric motion partition (AMP) out of which the decision of SMPs and AMPs are optimized in this paper. The key optimization techniques behind the proposed schemes are: 1) a conditional evaluation of the SMP modes; 2) range limitations primarily in the SMP sizes and secondarily in the AMP sizes; and 3) a selection of the SMP and AMP ranges as a function of the quantization parameter. These three techniques can be seamlessly incorporated in the existing control structures of the HEVC reference encoder without limiting its potential parallelization, hardware acceleration, or speed-up with other existing encoder optimizations. Our experiments show that the proposed schemes are able to cut the average complexity of the HEVC reference encoder by 31%-51% at a cost of 0.2%-1.3% bit rate increase under the random access coding configuration. The respective values under the low-delay B coding configuration are 32%-50% and 0.3%-1.3%.

3.1.2 4K Real-Time and Parallel Software Video Decoder for Multi-layer HEVC Extensions (2015)

At the moment of editing this report the paper has been accepted but it's not publicly available yet.
Two High Efficiency Video Coding (HEVC) extensions, namely the Scalable HEVC extension (SHVC) and the multi-view HEVC extension (MV-HEVC), have been finalized in July 2014 by the MPEG and VCEG. These two extensions enable additional features not covered in the first version of the HEVC standard such as: spatial, fidelity, bit depth and color gamut scalability, as well as stereoscopic and multi-view representations.
In this paper we propose a software parallel decoder architecture for the HEVC standard and its multi-layer extensions, including SHVC and MV-HEVC extensions. The decoder consists of multiple instances of the OpenHEVC decoder, one instance to decode each layer with a communication between dependent layers to perform inter-layer predictions. The proposed multi-layer HEVC decoder is parallel friendly and supports both wavefront parallelism to simultaneously process adjacent rows of the frame and frame-based parallelism to decode a set temporal and spatial frames in parallel. Moreover, the most time consuming operation introduced in the SHVC extension, namely the resampling of the inter-layer reference picture in spatial scalability, is optimized in SIMD for x86 platform.
We assess the complexity of the multi-layer HEVC decoder with respect to the simulcast configuration. The multi-layer decoder decoding two SHVC layers introduces in average 40%-71% additional complexity compared to the single layer HEVC decoder. Moreover, the low level optimizations with a hybrid parallel processing solution enable a real time decoding of 4Kp60 enhancement layer on a 6 cores Intel i7 processor running at 3.4 GHz.

3.2 IEEE Transactions on Consumer Electronics

3.2.1 Complexity analysis of an HEVC decoder based on a digital signal processor

High Efficiency Video Coding (HEVC) is a new video coding standard created by the JCT-VC group within ISO/IEC and ITU-T. HEVC is targeted to provide the same quality as H.264 at about half of the bit-rate and will replace soon to its predecessor in multimedia consumer applications. Up to now, only a few decoder implementations have been reported, most of them oriented to carry out a complexity analysis. In this paper, a DSP-based implementation of the HEVC HM9.0 decoder is presented. Up to the best of our knowledge, it is the first DSP-based implementation shown in the scientific literature. Several tests have been carried out to measure the decoder performance and the computational load distribution among its functional blocks. These results have been compared with the ones obtained with the decoder implementations reported up to date. Finally, based on the

results obtained in previous works regarding software optimization of DSP-based decoders, realtime could be achieved for SD formats with a single DSP after optimizing our HEVC decoder. For HD formats, multi-DSP technology will be needed.

3.2.2 A DSP-Based HEVC Decoder Implementation Using an Actor Language Dataflow Model

During the last decades, new video compression standards arose every few years with always higher compression gains and considerable increases on the computational cost. Single core processors have reached their limit and multicore processors are there to overcome this issue to give more processing power. In order to accelerate the implementation of new video coding standards, MPEG has standardized an alternative framework to describe video decoders. It is based on reference decoders written in the RVC CAL dataflow actor language. From these descriptions, a compiler – Open RVC CAL compiler (Orcc) – allows the automatic generation of C code dedicated to the target processor. In this paper, a DSP based decoder compliant with the new High Efficiency Video Coding (HEVC) standard has been implemented using a CAL RVC model as a starting point. This is the first implementation of an HEVC decoder with DSP technology based on a HEVC RVC CAL model. The decoder has been compared in performance with a GPP implementation, also based on the RVC CAL model, and outperforms it by more than 50%. Additionally, the performance of this decoder is compared with that of other DSP-based HEVC decoders implemented without using the Orcc infrastructure

3.2.3 A DSP HEVC decoder implementation based on openHEVC

The new High Efficiency Video Coding (HEVC) standard will replace H.264 soon in consumer multimedia applications. The open source project OpenHEVC is working on an efficient implementation of the HEVC decoder in C language. In this paper, an HEVC decoder based on OpenHEVC for DSP technology is presented. The tests show that it decodes about 2.3 times faster than a previously developed HM9.0-based decoder using the same DSP.

3.2.4 A multicore DSP HEVC decoder using an actor-based dataflow model and OpenMP

This paper explains how the Open Reconfigurable Video Coding CAL Actor Language compiler framework (Orcc) has been used, along with the Open Multi-Processing (OpenMP) API, to implement an HEVC video decoder based on multicore DSP technology. Currently, two DSP cores have been used, though the technique may be applied to the development of N-core based implementations. The two core based decoder presented in this paper outperforms a single core implementation by 70%.

3.2.5 Low power HEVC software decoder for mobile devices

In the context of mobile handheld devices, energy consumption is a primary concern and the process of video decoding is often among the most resource-intensive applications. Recent embedded processors are equipped with advanced features such as dynamic voltage frequency scaling (DVFS) in order to reduce their power consumption. These features can be used to perform low power video decoding when no hardware decoding support is available for a given standard. High efficiency video coding (HEVC) is a recent video standard offering state-of-the-art compression rates and advanced parallel processing solutions. This paper presents strategies for the power optimization of a real-time software HEVC decoder on NEON architecture. These strategies include the exploitation of data and task-level parallelism, as well as the use of a new frequency control system to optimize the processor DVFS, based on an estimation of the decoding complexity. Extensive power measurement results, based on a multi-core ARM big.LITTLE processor, are provided and compared to state-of-the-art. These results show that the proposed open-source implementation can reach an energy consumption below 21 nJ/px for HD decoding at 2.2 Mbits/s.

4 INTERNATIONAL CONFERENCES

4.1 ICCE 2014 - IEEE Conference on Consumer Electronics

4.1.1 On an implementation of HEVC video decoders with DSP technology

High Efficiency Video Coder (HEVC) will become a new MPEG International Standard by the end of 2012. HEVC is targeted to provide the same quality as H.264 at about a half of the bit-rate and will replace soon to its predecessor in multimedia consumer applications. In this paper, a preliminary implementation of an HEVC video decoder based on a DSP is presented and compared with a formerly developed H.264 DSP-based decoder.

4.1.2 A DSP HEVC decoder implementation based on OpenHEVC

The new High Efficiency Video Codec (HEVC) standard will replace H.264 soon in consumer multimedia applications. The open source project OpenHEVC is working on an efficient implementation of the HEVC decoder in C language. In this paper, an HEVC decoder based on OpenHEVC for DSP technology is presented. The tests show that it outperforms by 2.3 a previously developed HM9.0-based decoder for the same DSP.

4.2 ICASSP 2014 - IEEE International Conference on Acoustics, Speech, and Signal Processing

4.2.1 Multi-core software architecture for the scalable HEVC decoder

The scalable high efficiency video coding (SHVC) standard aims to provide features of temporal, spatial and quality scalability. In this paper we investigate a pipeline and parallel software architecture for the SHVC decoder. The proposed architecture is based on the OpenHEVC software which implements the high efficiency video coding (HEVC) decoder.
The architecture of the SHVC decoder enables two levels of parallelism. The first level decodes the base layer and the enhancement layers in parallel. The second level of parallelism performs the decoding of both the base layer and enhancement layers in parallel through the HEVC high level parallel processing solutions, including tile and wavefront. Up to the best of our knowledge, it is the first real time and parallel software implementation of the SHVC decoder. On an Intel Xeon processor running at 3.2 GHz, the SHVC decoder reaches the decoding of 1600p enhancement layer at 40 fps for x1.5 spatial scalability with using six concurrent threads.

4.3 DASIP 2014

4.3.1 MPEG high efficient video coding stream programming and many-cores scalability

MPEG High Efficient Video Coding (HEVC) is likely to emerge as the video coding standard for HD and Ultra-HD TV resolutions. The two elements that push HEVC beyond the previous standards are a higher compression efficiency of about a factor of two and the introduction of new coding tools (i.e. tiles and wavefront) that are intended to ease the largely increased encoding complexity (particularly for Ultra HD resolutions such as 4K and 8K). However, for HEVC decoder implementations, the achievement of the desired performance on massive parallel platforms cannot rely on the use of such optional (not enforced by MPEG profiles) tools. This work proposes a dataflow implementation of a HEVC decoder obtained using the standard language specified in ISO/IEC 23001-4. The objective of this work has been to maximize the algorithmic potential parallelism of the entire design and scale the implementation on a many core target architecture.

4.4 ICIP 2014 - IEEE International Conference on Image Processing

4.4.1 Exploring MPEG HEVC decoder parallelism for the efficient porting onto many-core platforms

MPEG High Efficient Video Coding (HEVC) is likely to emerge as the video coding standard for HD and Ultra-HD TV resolutions. The two elements that push HEVC beyond the previous standards are a higher compression efficiency of about a factor of two, and the introduction of new coding tools, tiles and wavefront that are intended to ease the largely increased encoding complexity particularly for Ultra HD resolutions such as 4K and 8K. However, for HEVC decoder implementations, the

achievement of the desired performance on massive parallel platforms cannot rely on the use of such optional (not enforced by MPEG profiles) tools. This paper reports results about the intrinsic parallelism of compliant HEVC decoding algorithms obtained by analyzing a dataflow implementation written using the standard language specified in ISO/IEC 23001-4 and structured attempting to maximize the algorithmic potential parallelism. The experimental results show what is the parallelism achieved by different dataflow architectures and how it can be further combined with the parallelism achieved by relying on tiles and wavefront, whenever they would be available, for porting a compliant HEVC decoder on massive parallel many-core platforms.

4.4.2 Real time SHVC decoder: implementation and complexity analysis

The Scalable High efficiency Video Coding (SHVC) standard is developed to offer spatial and quality scalability with high coding efficiency. In this paper we investigate a complexity analysis of a real time and parallel SHVC decoder. We first provide details on the implementation of the SHVC decoder including its low level optimizations. Furthermore, we introduce parallelism tools integrated in the SHVC software for parallel decoding. These tools include frame-based parallelism to decode a set of temporal and spatial frames in parallel as well as wavefront parallelism to simultaneously process separated regions of a picture. We assessed through experimental results the complexity of the real time SHVC decoder in different coding configurations. The SHVC decoder with two layers introduces in average an additional complexity of 43 to 80% in respect to a simulcast configuration. The low level optimizations together with a hybrid parallelism solution enable a real time decoding of 1600p40 enhancement layer on an Intel i7 processor.

4.5 ICME 2014 – IEEE Conference on Multimedia & Expo

4.5.1 Parallel SHVC decoder: implementation and analysis

The new Scalable High efficiency Video Coding (SHVC) standard is based on a multi-loop coding structure which requires the total decoding of all intermediate layers. The decoding complexity becomes then a real issue, especially for a real time decoding of ultra-high video resolutions.
A parallel processing architecture is proposed to reduce both the decoding time and the latency of the SHVC decoder. The proposed solution combines the high level parallel processing solutions defined in the HEVC standard with an extension of the frame-based parallelism. The latter solution enables the decoding of several spatial and temporal SHVC frames in parallel to enhance both decoding frame rate and latency. The wavefront parallel processing solution is used for more coarse level of granularity.
The proposed hybrid parallel processing approach achieves a near optimal speedup and provides a good trade-off between decoding time, latency and memory usage. On a 6 cores Xeon processor, the parallel SHVC decoder performs a real time decoding of 1600p60 video resolution.

4.6 SIPS 2014

4.6.1 Dataflow programs analysis and optimization using model predictive control techniques

This paper presents a new approach to buffer dimensioning for dynamic dataflow implementations. A novel transformation applied to the execution trace graph of a dataflow program is introduced in order to generate an event driven system. It is shown how model predictive control theory techniques can be applied to such a system to analyse the execution space of a dataflow program and to define and to minimize a bounded buffer size configuration that corresponds to a deadlock free execution. Some experimental results obtained using two design examples, i.e. a JPEG and an MPEG HEVC decoder, are reported and compared to the state of the art results in order to show the effectiveness of the introduced approach.

4.7 VCIP 2014

4.7.1 Comparative study of 8 and 10-bit HEVC encoders

This paper compares the rate-distortion-complexity (RDC) characteristics of the HEVC Main 10 Profile (M10P) and Main Profile (MP) encoders. The evaluations are performed with HEVC reference encoder (HM) whose M10P and MP are benchmarked with different resolutions, frame rates, and bit depths. The reported RD results are based on bit rate differences for equal PSNR whereas complexities have been profiled with Intel VTune on Intel Core 2 processor. With our 10-bit 4K 120 fps test set, the average bit rate decrements of M10P over MP are 5.8%, 11.6%, and 12.3% in the all-intra (AI), random access (RA), and low-delay B (LB) configurations, respectively. Decreasing

the bit depth of this test set to 8 lowers the RD gain of MI OP only slightly to 5.4% (AI), 11.4% (RA), and 12.1% (LB). The similar trend continues in all our tests even though the RD gain of M10P is decreased over MP with lower resolutions and frame rates. M10P introduces no computational overhead in HM, but it is anticipated to increase complexity and double the memory usage in practical encoders. Hence, the 10-bit HEVC encoding with 8-bit input video is the most recommended option if computation and memory resources are adequate for it.

4.8 IEEE Conference on Consumer Electronics

4.8.1 A multicore DSP HEVC decoder using an actor-based dataflow model

This paper explains how the Open Reconfigurable Video Coding CAL Actor Language compiler framework (Orcc) has been used, along with the Open Multi-Processing (OpenMP) API, to implement an HEVC video decoder based on multicore DSP technology. Currently, two DSP cores have been used, though the technique may be applied to the development of N-core based implementations. The two core based decoder presented in this paper outperforms a single core implementation by 70%.

4.9 IEEE International Symposium on Consumer Electronics 2015

4.9.1 A DSP based HEVC decoder implementation using RVC-CAL and native OpenHEVC code

Complexity of both applications and processors is permanently increasing while designers must face with a lot of challenges such as reduced time to market, performance and energy efficiency, among others. In this context, dataflow based methodologies and tools, like the Open RVC-CAL Compiler Infrastructure (Orcc), have revealed powerful in supporting platform independent design. Within the Orcc design flow, applications are described using the RVC-CAL language. A set of Orcc backends can generate different source codes (e.g., C, C++, VHDL, Java) that must be finally compiled for a target platform with a native compiler. This approach has several advantages, but the quality of the final product is limited by the quality of the currently implemented backends. In this work, an HEVC decoder implementation for DSP technology has been developed by using a combination of RVC-CAL descriptions and native C-code. The results of this approach are compared with those obtained by using both, a pure RVC-CAL description and a pure native C-code implementation.

4.10 ISCAS 2015

4.10.1 Kvazaar HEVC encoder for efficient intra coding

This paper presents an open-source Kvazaar encoder for HEVC intra coding. This academic software encoder has been developed from the scratch using C as an implementation language by prioritizing modularity, portability, and readability of the source code. Kvazaar implements almost the same intra coding functionality as HEVC reference encoder (HM) but its rewritten source code makes it significantly faster. In all-intra (AI) coding, a single-threaded C implementation of Kvazaar is 2.3 times faster than HM at a cost of 1.7% bit rate increase. The respective values with a high speed preset of Kvazaar are 10.6 and 8.8%. Compared to a single-threaded C++ implementation of x265, Kvazaar improves rate-distortion performance and increases encoding speed in both high-quality and high-speed test cases. Kvazaar has a particular edge in the high-speed test case where it almost halves the BD-rate loss and more than doubles the performance.

4.11 IEEE Globecom 2015

4.11.1 Network-assisted Multipath DASH Using the Distributed Decision Engine

At the moment of editing this report the paper is still under review.

4.12 SIPS 2015

4.12.1 Parallelization of Kvazaar HEVC intra encoder for multi-core processors

At the moment of editing this report the paper is still under review.

4.13 IEEE / ACM 1st International Workshop on Software Protection

4.13.1 Obfuscator-LLVM – Software Protection for the Masses

Software security with respect to reverse-engineering is a challenging discipline that has been researched for several years and which is still active. At the same time, this field is inherently

practical, and thus of industrial relevance: indeed, protecting a piece of software against tampering, malicious modifications or reverse-engineering is a very difficult task. In this paper, we present and discuss a software obfuscation prototype tool based on the LLVM compilation suite. Our tool is built as different passes, where some of them have been open-sourced and are freely available, that work on the LLVM Intermediate Representation (IR) code. This approach brings several advantages, including the fact that it is language-agnostic and mostly independent of the target architecture. Our current prototype supports basic instruction substitutions, insertion of bogus control-flow constructs mixed with opaque predicates, control-flow flattening, procedures merging as well as a code tamper-proofing algorithm embedding code and data checksums directly in the control-flow flattening mechanism.

4.14 Ciphertext-Policy Attribute-Based Broadcast Encryption with Small Keys

Broadcasting is a very efficient way to securely transmit information to a large set of geographically scattered receivers, and in practice, it is often the case that these receivers can be grouped in sets sharing common characteristics (or attributes). We describe in this paper an efficient ciphertext-policy attribute-based broadcast encryption scheme (CP-ABBE) supporting negative attributes and able to handle access policies in conjunctive normal form (CNF). Essentially, our scheme is a combination of the Boneh-Gentry-Waters broadcast encryption and of the Lewko-Sahai-Waters revocation schemes; the former is used to express attribute-based access policies while the latter is dedicated to the revocation of individual receivers. Our scheme is the first one that involves a public key and private keys having a size that is independent of the number of receivers registered in the system. Its selective security is proven with respect to the Generalized Diffie-Hellman Exponent (GDHE) problem on bilinear groups.

5 Other Publications

5.1 Media Synchronization Workshop 2013

5.1.1 Hybrid Broadcast Services using MPEG DASH

The emergence of new multimedia services such as super high definition or free viewpoint TV will put a very large bandwidth pressure on the broadcast networks. In order to offer these services while maintaining quality, service provider will have to use other delivery mechanisms. In this context, enhancing broadcast services with broadband media may be one key to low cost deployment of new services. This paper studies the problem of hybrid broadcast and broadband delivery of audio-visual content and reviews existing solutions. With the growing importance of HTTP streaming services, and the adoption of MPEG-DASH by the TV industry, a solution for hybrid broadcasting based on this standard is proposed. Implementation is presented and evaluated, and future work directions are discussed.

5.2 NAB Show 2014

5.2.1 4K Arrives! A Perspective from a Real UHDTV Broadcasting Experience

4K is certainly one of the last trending topics in the market and is called to be the engine of development in the broadcast industry for the coming years. However, several questions are still pending to solve not only from the technical but also from the commercial and strategic point of view. This paper describes the challenges that broadcast industry is facing for 4K to become a reality. In particular, key technologies such as the development of the new HEVC encoding and the new satellite transmission techniques will be presented along with other critical aspects for 4K quality assurance, such as frame rate, bit depth and color gamut. To support the analysis, the paper will present the real experience and field trials that Hipasat, together with a consortium of companies and with the collaboration of European projects H2B2VS and UHD4U, are carrying out for achieving an exciting milestone: the first HEVC 4K transmission with a bitrate bellow 20 Mbps, which is currently being broadcasted in Europe and in the near future, in North America and Latam over the Hispasat satellites. The attenders to this conference will have a clear insight about the commercial and technical requirements for 4K broadcasting included in the complete value chain (minimum bitrate, frame rate limitation, decoding capabilities, display features, etc) helping them to define the strategy and roadmap for their own 4K developments.

5.3 ESTIMedia 2013 Workshop

5.3.1 A DSP HEVC decoder implementation based on a RVC-CAL dataflow model

In this paper, a DSP-based decoder implementation compliant with the new HEVC standard is presented. The decoder has been designed by using a RVC-CAL dataflow model as a starting point. With the Orcc dataflow programming infrastructure, a C code has been generated from the RVC-CAL model. This code has been modified in order to be executed over a DSP. The decoder has been implemented and tested on a commercial development board. Up to the best of the authors' knowledge, this is the first DSP-based HEVC decoder implementation from a RVC-CAL model reported in the literature.
The decoder has been compared in performance with an ARM implementation, also based on the RVC-CAL model, and outperforms it by more than 50%. In addition, the decoder has been compared with other DSP-based HEVC decoders carried out in our previous work, one of them implemented from the HM9.0 reference software and the other from the open source code OpenHEVC. In these cases, the RVC-CAL based decoder is less efficient. Even so, RVC-CAL models will allow starting working over multicore platforms with important benefits exploiting parallelization processes.

5.4 Fourth W3C Web and TV Workshop

5.4.1 Hybrid Television - Use Cases and Business Models proposed by the H2B2VS project

This paper addresses the Use Cases and Business Models generated by the Celtic-PLUS H2B2VS project.
After a brief presentation of the project and its challenges, the different classes of Use Cases identified by H2B2VS are introduced. Business Models are then detailed and an association between the Use Cases and the Business Models is proposed.

5.5 Media Synchronization Workshop 2015

5.5.1 A Test Bed for Hybrid Broadcast Broadband Services

The users' demand for more content with more features have made broadcaster worldwide investigate how to enhance their broadcast services while not overloading their bandwidth capacities. This paper presents various use cases and a technical framework for experimenting with hybrid broadcast broadband delivery. This test bed can be reproduced from scratch using open source tools.

5.6 LP-EMS15

5.6.1 Energy Efficiency of a Parallel HEVC Software Decoder for Embedded Devices

In the context of fast adoption and deployment of recent video compression standard and thanks to recent high performance embedded processors, software video decoding can be performed in real time. But, it becomes among the most energy-intensive applications. Current embedded processors are based on multi-core architecture with advanced convenient features such as Dynamic Voltage Frequency Scaling (DVFS) in order to reduce their power consumption, allowing low power video decoding when no hardware decoding support is available for a given device. This paper deals with energy efficiency impact of different parallelization strategies of a software High Efficiency Video Coding (HEVC) decoder on multi-core ARM big.LITTLE processor. These strategies include the exploitation of data and task-level parallelism, as well as the use of different available DVFS policies.

5.7 IBC 2015

5.7.1 H2B2VS (HEVC hybrid broadcast broadband video services) – building innovative solutions over hybrid networks

Broadcast and broadband networks continue to be separate worlds in the video consumption business. Some initiatives such as HbbTV have built a bridge between both worlds, but its application is almost limited to providing links over the broadcast channel to content providers'

applications such as Catch-up TV services. When it comes to reality, the user is using either one network or the other.
H2B2VS is a Celtic-Plus project aiming at exploiting the potential of real hybrid networks by implementing efficient synchronization mechanisms and using new video coding standard such as High Efficiency Video Coding (HEVC). The goal is to develop successful hybrid network solutions that enable value added services with an optimum bandwidth usage in each network and with clear commercial applications. An example of the potential of this approach is the transmission of Ultra-HD TV by sending the main content over the broadcast channel and the required complementary information over the broadband network. This technology can also be used to improve the life of handicapped persons: Deaf people receive through the broadband network a sign language translation of a programme sent over the broadcast channel; the TV set then displays this translation in an inset window.
One of the most important contributions of the project is developing and testing synchronization methods between two different networks that offer unequal qualities of service with significant differences in delay and jitter.
In this paper, the main technological project contributions are described, including SHVC, the scalable extension of HEVC and a special focus on the synchronization solution adopted by MPEG and DVB. The paper also presents some of the implemented practical use cases, such as the sign language translation described above, and their performance results so as to evaluate the commercial application of this type of solution.