H2B2VS
D4.2.1

Publication Report

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EXECUTIVE SUMMARY

This deliverable provides a summary of all the publications produced by the project partners in relation to the project related activities. Publications include papers submissions to journals, international conferences, workshops and any other events publishing peer-reviewed proceedings.
This report provides a list of the publications with the relevant details and an abstract. All the papers are available for free download on the project web site: http://h2b2vs.epfl.ch
The document will be periodically updated with the new publications produced during the project lifetime.

Table of Contents

Table of Tables

1 DOCUMENT HISTORY AND ABBREVIATIONS

1.1 Document history

Version	Date	Description of the modifications
0.1	20/02/2014	First ToC
0.2	04/03/2014	Contributions and feedback from UPM, IETR, TVN
0.3	27/03/2014	Contribution from IETR

1.2 Abbreviations

DSP	Digital Signal Processor
HD	High Definition
HEVC	High Efficiency Video Coding
ICIP	Ieee International Conference on Image Processing
ICASSP	International Conference on Acoustics, Speech, and Signal Processing
ICCE	IEEE Conference on Consumer Electronics
NAB	National Association of Broadcasters
RVC	Reconfigurable Video Coding
SD	Standard Definition
SHVC	Scalable high efficiency video coding
TCSVT	Transactions on Circuits and Systems for Video Technology
UHD	Ultra High Definition

2 PUBLICATIONS SUMMARY

Journals	Title	Authors	Issue/Date	Status
IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS FOR VIDEO TECHNOLOGY (TCSVT)	EFFICIENT MODE DECISION SCHEMES FOR HEVC INTER PREDICTION	J. VANNE, M. VIITANEN, AND T. D. HÄMÄLÄINEN	FEBRUARY 2014	ACCEPTED
IEEE TRANSACTIONS ON CONSUMER ELECTRONICS	COMPLEXITY ANALYSIS OF AN HEVC DECODER BASED ON A DIGITAL SIGNAL PROCESSOR	PESCADOR, F.; CHAVARRIAS, M.; GARRIDO, M.J.; JUAREZ, E.; SANZ, C.	VOL. 59; ISSUE 2; PP. 391-399; MAY 2013	PUBLISHED
IEEE TRANSACTIONS ON CONSUMER ELECTRONICS	A DSP-BASED HEVC DECODER IMPLEMENTATION USING AN ACTOR LANGUAGE DATAFLOW MODEL	CHAVARRIAS, M.; PESCADOR, F. ; GARRIDO, M. ; JUÁREZ, E. ; RAULET, M.	VOL. 59; ISSUE 4; PP. 839-847; NOV 2013	PUBLISHED
IEEE TRANSACTIONS ON CONSUMER ELECTRONICS	A DSP HEVC DECODER IMPLEMENTATION BASED ON OPENHEVC	F. PESCADOR, J. P. CAÑO, M.J. GARRIDO, E. JUAREZ AND M. RAULET	TBD	IN PROGRESS
Conferences	**Title**	**Authors**	**Issue/Date**	
ICCE 2013 - IEEE CONFERENCE ON CONSUMER ELECTRONICS	ON AN IMPLEMENTATION OF HEVC VIDEO DECODERS WITH DSP TECHNOLOGY	PESCADOR, F.; GARRIDO, M.J.; JUAREZ, E.; SANZ, C.	JANUARY 2013, PP. 121-122	PUBLISHED
ICASSP 2014 – IEEE - INTERNATIONAL CONFERENCE ON ACOUSTICS, SPEECH, AND SIGNAL PROCESSING	MULTI-CORE SOFTWARE ARCHITECTURE FOR THE SCALABLE HEVC DECODER	HAMIDOUCHE W., RAULET, M., DEFORGES, O.	MAY 2014	ACCEPTED
ICCE 2014 - IEEE CONFERENCE ON CONSUMER ELECTRONICS	A DSP-BASED HEVC DECODER IMPLEMENTATION USING AN ACTOR LANGUAGE DATAFLOW MODEL	F. PESCADOR, J. P. CAÑO, M.J. GARRIDO, E. JUAREZ AND M. RAULET	JANUARY 2014, PP. 839 – 847	PUBLISHED
ICIP 2014 - IEEE INTERNATIONAL CONFERENCE ON IMAGE PROCESSING	EXPLORING MPEG HEVC DECODER PARALLELISM FOR THE EFFICIENT PORTING ONTO MANY-CORE PLATFORMS	D. DE SAINT JORRE, C. ALBERTI, M. MATTAVELLI, S. CASALE-BRUNET	TBD	SUBMITTED
ICME 2014 – IEEE CONFERENCE ON MULTIMEDIA & EXPO	PARALLEL SHVC DECODER: IMPLEMENTATION AND ANALYSIS	W. HAMIDOUCHE, M. RAULET AND OR D´EFORGES	JULY 14-18, 2014	ACCEPTED
Other Events	**Title**	**Authors**	**Issue/Date**	
NAB SHOW 2014	4K ARRIVES! A PERSPECTIVE FROM A REAL UHDTV BROADCASTING EXPERIENCE	MOURELLE, A.; RODRIGUEZ, J. ; SANZ, I.	9TH APRIL 2014	ACCEPTED
MEDIA SYNCHRONIZATION WORKSHOP 2013	HYBRID BROADCAST SERVICES USING MPEG DASH	JEAN LE FEUVRE AND CYRIL CONCOLATO	OCTOBER 29, 2013, NANTES, FRANCE	ACCEPTED
ESTIMEDIA 2013 WORKSHOP	A DSP HEVC DECODER IMPLEMENTATION BASED ON A RVC-CAL DATAFLOW MODEL	CHAVARRIAS, M.; PESCADOR, F. ; GARRIDO, M. ; JUÁREZ, E. ; RAULET, M.	--	NOT ACCEPTED
FOURTH W3C WEB AND TV WORKSHOP	HYBRID TELEVISION - USE CASES AND BUSINESS MODELS PROPOSED BY THE H2B2VS PROJECT	RAOUL MONNIER	12-13 MARCH 2014	ACCEPTED

Table 1- Summary of the H2B2VS publications

3 JOURNALS

3.1 IEEE Transactions on Circuits and Systems for Video Technology (TCSVT)

3.1.1 Efficient Mode Decision Schemes for HEVC Inter Prediction

At the moment of editing this document the paper has been accepted but it's not published yet.

3.2 IEEE Transactions on Consumer Electronics

3.2.1 Complexity analysis of an HEVC decoder based on a digital signal processor

High Efficiency Video Coding (HEVC) is a new video coding standard created by the JCT-VC group within ISO/IEC and ITU-T. HEVC is targeted to provide the same quality as H.264 at about half of the bit-rate and will replace soon to its predecessor in multimedia consumer applications. Up to now, only a few decoder implementations have been reported, most of them oriented to carry out a complexity analysis. In this paper, a DSP-based implementation of the HEVC HM9.0 decoder is presented. Up to the best of our knowledge, it is the first DSP-based implementation shown in the scientific literature. Several tests have been carried out to measure the decoder performance and the computational load distribution among its functional blocks. These results have been compared with the ones obtained with the decoder implementations reported up to date. Finally, based on the results obtained in previous works regarding software optimization of DSP-based decoders, realtime could be achieved for SD formats with a single DSP after optimizing our HEVC decoder. For HD formats, multi-DSP technology will be needed.

3.2.2 A DSP-Based HEVC Decoder Implementation Using an Actor Language Dataflow Model

During the last decades, new video compression standards arose every few years with always higher compression gains and considerable increases on the computational cost. Single core processors have reached their limit and multicore processors are there to overcome this issue to give more processing power. In order to accelerate the implementation of new video coding standards, MPEG has standardized an alternative framework to describe video decoders. It is based on reference decoders written in the RVC CAL dataflow actor language. From these descriptions, a compiler – Open RVC CAL compiler (Orcc) – allows the automatic generation of C code dedicated to the target processor. In this paper, a DSP based decoder compliant with the new High Efficiency Video Coding (HEVC) standard has been implemented using a CAL RVC model as a starting point. This is the first implementation of an HEVC decoder with DSP technology based on a HEVC RVC CAL model. The decoder has been compared in performance with a GPP implementation, also based on the RVC CAL model, and outperforms it by more than 50%. Additionally, the performance of this decoder is compared with that of other DSP-based HEVC decoders implemented without using the Orcc infrastructure

3.2.3 A DSP HEVC decoder implementation based on openHEVC

At the moment of editing this document, the work on this paper is in progress.

4 INTERNATIONAL CONFERENCES

4.1 ICCE 2014 - IEEE Conference on Consumer Electronics

4.1.1 On an implementation of HEVC video decoders with DSP technology

High Efficiency Video Coder (HEVC) will become a new MPEG International Standard by the end of 2012. HEVC is targeted to provide the same quality as H.264 at about a half of the bit-rate and will replace soon to its predecessor in multimedia consumer applications. In this paper, a preliminary implementation of an HEVC video decoder based on a DSP is presented and compared with a formerly developed H.264 DSP-based decoder.

4.1.2 A DSP HEVC decoder implementation based on OpenHEVC

The new High Efficiency Video Coding (HEVC) standard will replace H.264 soon in consumer multimedia applications. The open source project OpenHEVC is working on an efficient implementation of the HEVC decoder in C language. In this paper, an HEVC decoder based on OpenHEVC for DSP technology is presented. The tests show that it decodes about 2.3 times faster than a previously developed HM9.0-based decoder using the same DSP

4.2 ICIP 2014 - IEEE International Conference on Image Processing

4.2.1 Exploring MPEG HEVC decoder parallelism for the efficient porting onto many-core platforms

At the moment of editing this document, this paper has been submitted for review.

4.3 ICASSP 2014 - IEEE International Conference on Acoustics, Speech, and Signal Processing

4.3.1 Multi-core software architecture for the scalable HEVC decoder

The scalable high efficiency video coding (SHVC) standard aims to provide features of temporal, spatial and quality scalability. In this paper we investigate a pipeline and parallel software architecture for the SHVC decoder. The proposed architecture is based on the OpenHEVC software which implements the high efficiency video coding (HEVC) decoder.
The architecture of the SHVC decoder enables two levels of parallelism. The first level decodes the base layer and the enhancement layers in parallel. The second level of parallelism performs the decoding of both the base layer and enhancement layers in parallel through the HEVC high level parallel processing solutions, including tile and wavefront. Up to the best of our knowledge, it is the first real time and parallel software implementation of the SHVC decoder. On an Intel Xeon processor running at 3.2 GHz, the SHVC decoder reaches the decoding of 1600p enhancement layer at 40 fps for x1.5 spatial scalability with using six concurrent threads.

4.4 ICME 2014 – IEEE Conference on Multimedia & Expo

4.4.1 Parallel SHVC decoder: implementation and analysis

The new Scalable High efficiency Video Coding (SHVC) standard is based on a multi-loop coding structure which requires the total decoding of all intermediate layers. The decoding complexity becomes then a real issue, especially for a real time decoding of ultra-high video resolutions.
A parallel processing architecture is proposed to reduce both the decoding time and the latency of the SHVC decoder. The proposed solution combines the high level parallel processing solutions defined in the HEVC standard with an extension of the frame-based parallelism. The latter solution enables the decoding of several spatial and temporal SHVC frames in parallel to enhance both decoding frame rate and latency. The wavefront parallel processing solution is used for more coarse level of granularity.
The proposed hybrid parallel processing approach achieves a near optimal speedup and provides a good trade-off between decoding time, latency and memory usage. On a 6 cores Xeon processor, the parallel SHVC decoder performs a real time decoding of 1600p60 video resolution.

5 OTHER PUBLICATIONS

5.1 Media Synchronization Workshop 2013

5.1.1 Hybrid Broadcast Services using MPEG DASH

The emergence of new multimedia services such as super high definition or free viewpoint TV will put a very large bandwidth pressure on the broadcast networks. In order to offer these services while maintaining quality, service provider will have to use other delivery mechanisms. In this context, enhancing broadcast services with broadband media may be one key to low cost deployment of new services. This paper studies the problem of hybrid broadcast and broadband delivery of audio-visual content and reviews existing solutions. With the growing importance of HTTP streaming services, and the adoption of MPEG-DASH by the TV industry, a solution for hybrid broadcasting based on this standard is proposed. Implementation is presented and evaluated, and future work directions are discussed.

5.2 NAB Show 2014

5.2.1 4K Arrives! A Perspective from a Real UHDTV Broadcasting Experience

4K is certainly one of the last trending topics in the market and is called to be the engine of development in the broadcast industry for the coming years. However, several questions are still pending to solve not only from the technical but also from the commercial and strategic point of view. This paper describes the challenges that broadcast industry is facing for 4K to become a reality. In particular, key technologies such as the development of the new HEVC encoding and the new satellite transmission techniques will be presented along with other critical aspects for 4K quality assurance, such as frame rate, bit depth and color gamut. To support the analysis, the paper will present the real experience and field trials that Hipasat, together with a consortium of companies and with the collaboration of European projects H2B2VS and UHD4U, are carrying out for achieving an exciting milestone: the first HEVC 4K transmission with a bitrate bellow 20 Mbps, which is currently being broadcasted in Europe and in the near future, in North America and Latam over the Hispasat satellites. The attenders to this conference will have a clear insight about the commercial and technical requirements for 4K broadcasting included in the complete value chain (minimum bitrate, frame rate limitation, decoding capabilities, display features, etc) helping them to define the strategy and roadmap for their own 4K developments.

5.3 ESTIMedia 2013 Workshop

5.3.1 A DSP HEVC decoder implementation based on a RVC-CAL dataflow model

In this paper, a DSP-based decoder implementation compliant with the new HEVC standard is presented. The decoder has been designed by using a RVC-CAL dataflow model as a starting point. With the Orcc dataflow programming infrastructure, a C code has been generated from the RVC-CAL model. This code has been modified in order to be executed over a DSP. The decoder has been implemented and tested on a commercial development board. Up to the best of the authors' knowledge, this is the first DSP-based HEVC decoder implementation from a RVC-CAL model reported in the literature.
The decoder has been compared in performance with an ARM implementation, also based on the RVC-CAL model, and outperforms it by more than 50%. In addition, the decoder has been compared with other DSP-based HEVC decoders carried out in our previous work, one of them implemented from the HM9.0 reference software and the other from the open source code OpenHEVC. In these cases, the RVC-CAL based decoder is less efficient. Even so, RVC-CAL models will allow starting working over multicore platforms with important benefits exploiting parallelization processes.

5.4 Fourth W3C Web and TV Workshop

5.4.1 Hybrid Television - Use Cases and Business Models proposed by the H2B2VS project

At the moment of editing this document the actual content of the presentation is under review.